REMARKS

The specification has been amended on pages 1 and 2 to remove references to the claims.

The claims have been amended to more clearly define the invention as disclosed in the written description. In particular, claim 2 has been cancelled, while claims 1 and 7 have been amended to include the limitations of cancelled claim 2. In addition, the claims have been amended for clarity.

Applicants believe that the above changes answer the Examiner's objections to the specification, the Examiner's 35 U.S.C. 112, paragraphs 1 and 2, rejections of claims 1-7, and the Examiner's 35 U.S.C. 101 rejection of claims 1-6, and respectfully request withdrawal thereof.

The Examiner has rejected claims 1-7 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 5,754,764 to Davis et al.

The Davis et al. patent discloses a combination of input output circuitry and local area network systems, in which memory mapping is performed, and in which multicasting is also performed.

As noted in MPEP § 2131, it is well-founded that "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California,* 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Further, "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v.*

Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Claim 1 includes the limitation "the network is arranged to establish transactions between a first electronic module and at least two second electronic modules". The Examiner has indicated that this limitation is taught by Davis et al. at col. 3, lines 22-45, col. 15, lines 19-60 and col. 27, lines 38-40.

Applicants believe that the Examiner is mistaken. In particular, Davis et al., at col. 3, lines 22-45, states :

> "The receive buffer is positioned in a physical memory, which has a size, that is reduced by a memory mapping subsystem. The memory mapping subsystem maps the receive buffer ("original--logical") into a physical buffer ring. The memory mapping subsystem has a set of physical address registers and pointers. The pointers control data read and data write operations to the physical buffer. In addition, the memory mapping subsystem comprises a memory array ("address translation table") to correlate the physical address to an address in the receive buffer. The memory array holds at least one physical address. The physical address(es) are selected from the group consisting of beginning location of the data packet(s), current packet pointer, and boundary packet pointer. The memory mapping subsystem is preferably a circuit and operates automatically when the receive buffer is utilized. The receive and transmit buffers have a variable size. The data packet(s) are stored in the receive buffer immediately after one another. The memory mapping subsystem translates at least one address referencing data in the physical memory to an at least one address in a logical memory. In addition, the preferred memory mapping system comprises a network interface controller system. The network interface controller system comprises a physical remote address register to remote dma read from a first buffer only..."

and at col. 27, lines 38-40 states:

> "Ethernet controller module 6 reads the first 8 words from the E.sup.2 PROM and maps them into the memory map at the appropriate address."

Col. 15, lines 19-60 contains various tables showing parallel port addresses, and COM port selections.

Applicants submit that it should be apparent from the above that Davis et al. does not show "the network is arranged to establish transactions between a first electronic module and at least two second electronic modules".

The subject invention, as claimed in claim 1, further includes the limitation "means for replicating a single request from the first electronic module into at least two replicated requests". The Examiner has indicated that this is taught by Davis et al. at col. 27, lines 38-40 and col. 51, lines 22-42.

While Davis et al. describes multicast address registers at the col. 51 location, there is no disclosure that the Davis et al. system actually replicates a single request into at least two replicated requests.

The Examiner has stated "It is inherent in multicasting that the message to be multicast are replicated accordingly." However, Applicants submit that the Examiner has not shown any indication in Davis et al. or any other prior art reference to support such a statement.

In view of the above, Applicants believe that the subject invention, as claimed, is neither anticipated nor rendered obvious by the prior art, and as such, is patentable thereover.

Applicants believe that this application, containing claims 1 and 3-7, is now in condition for allowance and such action is respectfully requested.

Respectfully submitted,

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